Xuehai Qian

CONTACT INFORMATION

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RESEARCH INTERESTS

Computer architecture.
System and architecture for graph processing and machine learning.
Hardware acceleration with emerging technologies

EDUCATION

- **University of Illinois at Urbana-Champaign (UIUC)** — Urbana, IL
  Ph.D. in Computer Science (with Prof. Josep Torrellas) — Aug. 2007 – Aug. 2013
  • Dissertation title: *Scalable and Flexible Bulk Architecture*
- **Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS)** — Beijing
  M.S. in Computer Engineering — Sept. 2004 – Jul. 2007
- **Beihang University (BUAA)** — Beijing
  B.S. in Computer Engineering (with honor) — Sept. 2000 – Jul. 2004

PROFESSIONAL EXPERIENCE

- Assistant Professor, *University of Southern California.* — Aug. 2015 – Present
- Postdoctoral Researcher, *UC Berkeley.* — Sept. 2013 – June 2015
- Research Intern, *Microsoft Research, Silicon Valley* — Summer 2011
- Research Intern, *Microsoft Research, Redmond* — Summer 2008

AWARDS AND HONORS

- **O**ne of 200 selected to participate Heidelberg Laureate Forum Foundation (HLFF) — 2015
- **W**.J. Poppelbaum Memorial Award, UIUC — 2013
- **N**ominated for an IBM Ph.D. Fellowship, UIUC — 2011
- **N**ominated for a Microsoft Research Ph.D. Fellowship, UIUC — 2008
- **A**ndrew and Shana Laursen Fellowship, UIUC — 2007
- **O**utstanding Master's Thesis Award, ICT, CAS — 2007
- **N**OKIA Fellowship, ICT, CAS — 2007
- **O**utstanding Bachelor's Thesis Award, Beihang University — 2004
- **Q**IAN Changzhao Award, Beihang University — 2003
  Awarded to the top computer science student.

PUBLICATIONS

- Mengxing Liu, Mingxing Zhang, Kang Chen, **Xuehai Qian**, Yongwei Wu, Weimin Zheng and Jinglei Ren. *DudeTX: Durable Decoupled Transaction*. To appear in **ACM Transactions on Storage**.
- Caiwen Ding, Yanzhi Wang, Siyu Liao, Zhe Li, Yu Bai, Youwei Zhuo, Chao Wang, **Xuehai Qian**, Ning Liu, Geng Yuan, Xiaolong Ma, Yipeng Zhang, Xue Lin, Jian Tang, Qinru Qiu, Bo Yuan. *Cir-CNN: Accelerating and Compressing Deep Neural Networks Using Block-Circulant Weight Matrices*. **MICRO'17**
- Zhiyuan Ai, Mingxing Zhang, Yongwei Wu, **Xuehai Qian**, Kang Chen, Weimin Zheng *Squeezing out All the Value of Loaded Data: An Out-Of-Core Graph Processing System with Reduced Disk I/O*. **ATC'17**
- Abdulaziz Tabbakh, Murali Annavaram and **Xuehai Qian** *Power Efficient Sharing-Aware GPU Data Management* . **IPDPS'17**
- Ao Ren, Ji Li, Zhe Li, Caiwen Ding, **Xuehai Qian**, Qinru Qiu, Bo Yuan and Yanzhi Wang *SC-DCNN: Highly-Scalable Deep Convolutional Neural Network using Stochastic Computing*. **ASPLOS'17**

- Mengxing Liu, Mingxing Zhang, Kang Chen, **Xuehai Qian**, Yongwei Wu, Weimin Zheng and Jinglei Ren. *DudeTM: Building Durable Transactions for Persistent Memories with Decoupling*. **ASPLOS'17**
- Linghao Song, **Xuehai Qian**, Hai Li and Yiran Chen *PipeLayer: A Pipelined ReRAM-Based Accelerator for Deep Learning*. **HPCA'17**
- Mingxing Zhang, Yongwei Wu, Kang Chen, **Xuehai Qian**, Xue Li and Weimin Zheng *Exploring the Hidden Dimension in Graph Processing*. **OSDI'16**
- **Xuehai Qian**, Koushik Sen, Paul Hargrove and Costin Iancu. *SReplay: Deterministic Group Replay for One-Sided Communication*. **ICS'16**
- Hui Wang, Rui Wang, Zhongzhi Luan, **Xuehai Qian** and Depei Qian. *Improving Multiprocessor Performance with Fine-grain coherence bypass*. **SCIENCE CHINA Information Sciences** 58(1), 2015.
- **Xuehai Qian**, Benjamin Sahelices and Depei Qian. *Pacifier: Record and Replay for Relaxed-Consistency Multiprocessors with Distributed Directory Protocol*. **ISCA'14**
- **Xuehai Qian**, Benjamin Sahelices and Josep Torrellas. *OmniOrder: Directory-Based Conflict Serialization of Transactions*. **ISCA'14**
- **Xuehai Qian**, Benjamin Sahelices, Josep Torrellas and Depei Qian. *BulkCommit: Scalable and Fast Commit of Atomic Blocks in a Lazy Multiprocessor Environment*. **MICRO'13**
- **Xuehai Qian**, Benjamin Sahelices, Josep Torrellas and Depei Qian. *Volition: Precise and Scalable Sequential Consistency Violation Detection*. **ASPLOS'13**
- **Xuehai Qian**, He Huang, Benjamin Sahelices, and Depei Qian. *Rainbow: Efficient Memory Dependence Recording with High Replay Parallelism for Relaxed Memory Model*. **HPCA'13**
- **Xuehai Qian**, Benjamin Sahelices and Josep Torrellas. *BulkSMT: Designing SMT Processors for Atomic-Block Execution*. **HPCA'12**
- **Xuehai Qian**, Wonsun Ahn and Josep Torrellas. *ScalableBulk: Scalable Cache Coherence for Atomic Blocks in a Lazy Environment*. **MICRO'10**
- **Xuehai Qian**, He Huang, Zhenzhong Duan, Junchao Zhang, Nan Yuan, Yongbin Zhou, Hao Zhang, Huimin Cui and Dongrui Fan. *Optimized Register Renaming Scheme for Stack-based x86 Floating Point Operations*. **ARCS'07**
- **Xuehai Qian**, He Huang, Hao Zhang, Junchao Zhang and Dongrui Fan. *Design and Implementation of Floating Point Stack on General RISC Architecture*. **PDP'07**
- **Xuehai Qian**, Hao Zhang, Jingang Yang, He Huang, Junchao Zhang and Dongrui Fan. *Circuit Implementation of Floating Point Range Reduction for Trigonometric Functions*. **ISCAS'07**

TALKS

- *Graph Processing System and Architecture*
  – Brown University, Oct. 2017
- *Reducing Data Movements in Graph Processing: from Distributed System to Emerging Technology* –
  University of Texas, Austin, Feb. 2017
  – Rice University, Feb. 2017
  – Cornell University, Dec. 2016
  – University of Illinois, Urbana-Champaign, Dec. 2016
  – University of Pennsylvania, Dec. 2016
  – VMware Research, Dec. 2016
  – Google, Dec. 2016
  – University of California, Santa Barbara, Jan. 2017
- *Breaking the Myth of "Think as a Vertex".*
  – University of California, Irvine, Oct. 2016
- *Taming Relaxed-Consistency and Non-determinism in Parallel Systems.*
  – CALCM Seminar, Carnegie Mellon University, Jan. 2015.
  – Georgia Tech, Jan. 2015.
  – University of Pennsylvania, Feb. 2015
  – Syracuse University, Feb. 2015

– Purdue University (CS), Feb. 2015
– University of California Riverside, Mar. 2015
– University of Virginia, Mar. 2015
– Boston University, Mar. 2015
– University of Southern California, Mar. 2015
– Purdue University (ECE), Mar. 2015

- *Clearing Chaos: Taming Relaxed-Consistency in Multiprocessors.*
  – Intel Labs, Santa Clara, Jun. 2014.
  – AMD Research, Sunnyvale, Jun. 2014.
- *Scalable and Flexible Bulk Architecture.*
  – CECA, Peking University, Dec. 2012.
  – University at Buffalo, The State University of New York, Feb. 2013.
  – Washington University in St. Louis, Feb. 2013.
  – IIIS, Tsinghua University, Feb. 2013.
  – Rutgers University, Mar. 2013.
  – Florida International University, Mar. 2013.
  – Penn State University, Mar. 2013.
  – The George Washington University, Mar. 2013.
  – Oracle, Apr. 2013.
  – Drexel University, Apr. 2013.
  – Microsoft Research, Asia (MSRA), May. 2013.
  – The University of Edinburgh, May. 2013.
  – The University of Manchester, May. 2013.
  – AMD Research Lab, June. 2013.
  – UC Berkeley, Jun. 2013.
  – Intel Labs, Santa Clara, Dec. 2013.

SERVICE

PC member of HPCA 2018, ISCA 2017, SOCC 2017, HiPC 2017, ICPP 2016, IPDPS 2015, HiPC 2016.

External Review Committee of MICRO 2017, ASPLOS 2017, HPCA 2017, MICRO 2016, MICRO 2015, PACT 2016.

Submission Co-chair of ISCA 2012.

Publication Chair of HPCA 2017.

Travel Grant Chair of ASPLOS 2017.

Web Co-Chair of ASPLOS 2018.

Local Arrangement Chair of ISCA 2018. 2012.
Reviewer for ISCA, MICRO, PLDI, ASPLOS, HPCA, PPOPP, SC, IPDPS.
IEEE Transactions on Very Large Scale Integration Systems.
IEEE Transactions on Parallel and Distributed Systems.
IEEE Transactions on Computers.
IEEE Computer Architecture Letters.
ACM Transactions on Design Automation of Electronic Systems.
ACM Transactions on Computer Architecture and Code Optimization.
IEEE MICRO.
Concurrency and Computation: Practice and Experience.

Organizer of Computer Engineering Seminar at USC.

Member of IEEE and ACM.

GRANTS

CRII: SHF: Improving Programmability of GPGPU/NVRAM Integrated Systems with Holistic Architectural Support (CCF-1657333), $175,000.

SHF: Small: Accelerating Graph Processing with Vertically Integrated Programming Model, Runtime and Architecture (CCF-1717754), $450,000.

CSR: Small: Collaborative Research: GAMBIT: Efficient Graph Processing on a Memristor-based Embedded Computing Platform (CNS-1717984), $250,000.